WHAT IS CLAIMED IS:

1. A method of creating a ROM soft IP comprising the steps of:

(a) preparing a head file which describes the initial information of the ROM soft IP in a given electronic circuit design language, a tail file which describes the end information of the ROM soft IP in the given electronic circuit language, and an empty ROM soft IP file , and selecting a hex file for an MPU program memory, which includes a start address (s) and an instruction (s) composed of ASCII characters; and

(b) copying the head file into the first part of the empty ROM soft IP file, converting the hex file for the MPU program memory into the given electronic circuit design language expression and writing the converted expression into the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file.

2. The method of creating the ROM soft IP according to claim 1, wherein the procedure of converting the hex file for the MPU program memory into the given electronic circuit design language expression in the step (b) is performed by analyzing the start address (s) and the instruction (s) in the hex file and transforming them into binary codes, respectively.

3. The method of creating the ROM soft IP according to claim 1, wherein the ROM soft IP is described in any one of the electronic circuit design languages including very high speed description language (VHDL) and Verilog.

4. The method of creating the ROM soft IP according to claim 1, wherein the ROM soft IP can be built in the MPU instead of a mask ROM.

5. The method of creating the ROM soft IP according to claim 1, wherein the head file has the initial information including a library to be applied to the IP, the name of the IP, and an input/output signal, and the statement for describing the ROM address and the instruction at the address, the initial information and the statement being described in the electronic circuit design language, and

the tail file has last data of the ROM and an end statement described in the electronic circuit design language.

6. The method of creating the ROM soft IP according to claim 1, wherein the procedure of converting the instruction into the electronic circuit design language in the step (b) is performed by describing the number of the instructions of the hex file composed of ASCII characters in a decimal by using a function converting a character into an integer.

7. The method of creating the ROM soft IP according to claim 1, wherein the ROM soft IP described in the electronic circuit design language is incorporated with an MPU core IP and is built-in as an accessory.

8. The method of creating the ROM soft IP according to claim 7,

further comprising the step of incorporating the ROM soft IP with the MPU core IP and performing circuit synthesizing and verifying procedures by a CAD tool.

9. A computer readable recording media having a program for executing a method of creating a ROM soft IP the steps of:

(a) preparing a head file which describes the initial information of the ROM soft IP in a given electronic circuit design language, a tail file which describes the end information of the ROM soft IP in the given electronic circuit language, and an empty ROM soft IP file, and selecting a hex file for an MPU program memory, which includes a start address (s) and an instruction (s) composed of ASCII characters; and

(b) copying the head file into the first part of the empty ROM soft IP file, converting the hex file for the MPU program memory into the given electronic circuit design language expression and writing the converted expression into the middle part of the ROM soft IP file, and copying the tail file into the last part of the ROM soft IP file.

10. The computer readable recording media according to claim 9, wherein the procedure of converting the hex file for the MPU program memory into the given electronic circuit design language expression in the step (b) is performed by analyzing the start address (s) and the instruction (s) in the hex file and transforming them into binary codes, respectively.

11. The computer readable recording media according to claim 9, wherein the ROM soft IP is described in any one of the electronic circuit design languages including very high speed description language (VHDL) and Verilog.

12. The computer readable recording media according to claim 9, wherein the ROM soft IP can be built in the MPU instead of a mask ROM.

13. The computer readable recording media according to claim 9, wherein the head file has the initial information including a library to be applied to the IP, the name of the IP, and an input/output signal, and the statement for describing the ROM address and the instruction at the address, the initial information and the statement being described in the electronic circuit design language, and

the tail file has last data of the ROM and an end statement described in the electronic circuit design language.

14. The computer readable recording media according to claim 9, wherein the procedure of converting the instruction into the electronic circuit design language in the step (b) is performed by describing the number of the instructions of the hex file composed of ASCII characters in a decimal by using a function converting a character into an integer.

15. The computer readable recording media according to claim 9, wherein the ROM soft IP described in the electronic circuit design language is incorporated with an MPU core IP and is built-in as an accessory.

16. The computer readable recording media according to claim 9, further comprising the step of incorporating the ROM soft IP with the MPU core IP and performing circuit synthesizing and verifying procedures by a 6CAD tool.